Notice of Allowability	Application No.	Applicant(s)	
	10/038,159	CASPER, BRYAN K.	
	Examiner	Art Unit	
	Daniel Swerdlow	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *interview of 22 July 2005*.

2. ☒ The allowed claim(s) is/are *1,5-18 and 20*.

3. ☒ The drawings filed on *02 January 2002* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An extension of time under 37 CFR 1.136(a) is required in order to make an examiner's amendment which places this application in condition for allowance. During a telephone conversation conducted on 3 August 2005, Mr. Farzad E. Amini, reg. no. 42,261 requested an extension of time for 1 MONTH(S) and authorized the Director to charge Deposit Account No. 02-2666 the required fee of $120 for this extension and authorized the following examiner's amendment. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Farzad E. Amini, reg. no. 42,261 on 22 July 2005.

The application has been amended as follows:

Claim 1 is amended to read as follows:

1. (Currently Amended) A circuit comprising:

an echo cancellation circuit in which a comparator has [[an]] <u>a differential</u> input coupled

to receive a differential transmission line analog signal level, the comparator having a discrete time variable offset that is controllable via an offset control input to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the differential transmission line analog signal level and the variable reference level; and

a driver on the same integrated circuit die as the echo cancellation circuit and coupled to transmit driver data symbols,

and wherein the echo cancellation circuit further includes a discrete time echo cancellation filter whose input is coupled to receive the driver data symbols and whose output is coupled to [[an]] the offset control input of the comparator.

Claim 5 is amended to read as follows:

5. (Currently Amended) The circuit of claim 1 further comprising a sample and hold circuit whose output is coupled to provide the differential transmission line analog signal level to the comparator.

Claim 6 is amended to read as follows:

6. (Currently Amended) The circuit of claim 1 wherein the comparator [has a]] differential input is provided by first and second differential pairs each being intentionally unbalanced, each pair having first and second output nodes, the first output node of the first pair being coupled to the second output node of the second pair, the second output node of the first pair being coupled to the first output node of the second pair, and first and second variable

current generators coupled to control respective tail currents of the first and second differential pairs.

Claim 8 is amended to read as follows:

8. (Currently Amended) A method comprising:

determining a binary value based on a sequence of data symbols that have been transmitted by a near end driver in a communication link, the binary value being one of a plurality of binary values that are designed to increase a voltage margin of a near end receiver in the presence of echo in the communication link; and

applying the binary value to an offset control input of a comparator in the near end receiver, and applying a differential transmission line analog signal level of the communication link to [[an]] a differential input of the comparator, the comparator having a variable offset that is controllable, via the offset control input, to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the differential transmission line analog signal level and the variable reference level.

Claim 13 is amended to read as follows:

13. (Currently Amended) A system comprising:

a printed wiring board on which a bus is formed, an integrated circuit (IC) chip package being operatively installed on the board to communicate using the bus, the package having an IC chip that includes a logic function section and an I/O section as an interface between the logic function section and the bus, the I/O section having a bus receiver in which an echo cancellation

circuit includes a comparator that has [[an]] a differential input to receive a differential bus analog signal level, the comparator having a variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the differential bus analog signal level and the variable reference level, wherein the comparator [[has a]] differential input is provided by first and second differential pairs each being intentionally unbalanced, each pair having first and second output nodes, the first output node of the first pair being coupled to the second output node of the second pair, the second output node of the first pair being coupled to the first output node of the second pair and first and second variable current generators coupled to control respective tail currents of the first and second differential pairs.

Claim 18 is amended to read as follows:

18. (Currently Amended) An article of manufacture comprising:

a machine-readable medium having instructions stored thereon which, when executed by a processor, cause an electronic ~~system to display a representation of~~ design automation tool to simulate an echo cancellation circuit in which a comparator has [[an]] a differential input to receive a differential transmission line analog signal level, the comparator having a variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the differential transmission line analog signal level and the variable reference level, a driver on the same integrated circuit die as the echo cancellation circuit and coupled to transmit driver data symbols received at its input and wherein ~~the representation of~~ the echo cancellation circuit includes a discrete time echo

cancellation filter whose input is coupled to receive the driver data symbols and whose output is coupled to a discrete time offset control input of the comparator.

Claim 20 is amended to read as follows:

20. (Currently Amended) The article of manufacture of claim 18 wherein the ~~representation of the~~ comparator includes first and second differential transistor pairs each being intentionally unbalanced, each pair having first and second output nodes, the first output node of the first pair being coupled to the second output node of the second pair, the second output node of the first pair being coupled to the first output node of the second pair, and first and second variable current generators coupled to control respective tail currents of the first and second differential pairs.

3. The following is an examiner's statement of reasons for allowance:

4. Claims 1, 8, and 13 are patentably distinct from US Patent 6,344,756 to Cecchi for reasons stated in the prior Office action mailed on 26 April 2005.

5. Regarding Claim 1, US Patent 4,748,66 to Pope discloses an echo canceller (Figure) that combines a discrete time variable offset (d_k) with an echo replica (y_k) formed by an echo cancellation filter (4) from driver data symbols (1) and subtracts the combined signal (x_k) from a transmission line analog signal (z_k). Pope further discloses a driver (2) that transmits the driver data symbols. However, Pope does not disclose a comparator with a differential input receiving a differential transmission line signal or the output of the echo cancellation filter coupled to an

offset control input of the comparator. As such, Pope neither anticipates nor suggests the claimed invention.

6. Claims 8 and 13 recite limitations essentially similar to those of Claim 1 and are patentably distinct from Pope for the same reasons.

7. Claim 18 is amended to recite that the instructions on the machine-readable medium cause an electronic design tool to simulate the patentable echo cancellation circuit. Because the instructions actually result in a simulation, as opposed to a mere display of a representation of a circuit, the limitations directed to the structure of the echo cancellation circuit are functional rather than merely descriptive and are given weight. As such, Claim 18 is allowable for reasons stated above apropos of Claim 1.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 571-272-7531. The examiner can normally be reached on Monday through Friday between 7:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh H. Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Swerdlow
Examiner
Art Unit 2646

ds
27 July 2005